Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

CLAIMS

1.   (currently amended) A method of producing [[a]]one or more packetized signals from one or more input signals comprising:

    (a)   receiving a plurality ofone or more input signals;

    (b)   buffering each of the input signals in a memory system;

    (c)   processing at least one of the input signals to provide a processed signal and buffering the processed signal in the memory system;

    (d)(c) designating at least some of the input signals or the processed signals as packet source signals and assigning each of the packet source signals a unique global identification code; and

    (e)(d) retrieving at least one of theone or more of the packet source signals and generating the one or more packetized signals wherein each of the packetized signals includes a series of packetized signal packets, wherein each of the packetized signal packets contains the unique global identification code of one of the packet source signals and data corresponding to the same packet source signal,

    wherein each of the one or more packetized signals may be further processed using the unique global identification code of each packetized signal packet to produce one or more output signals.

2.   (currently amended) The method of claim 1 wherein each of packet source signals comprises a series of packet source signal packets, and wherein each of the packetized signal packets is formed by retrieving one or more the packet source signal packets corresponding to a single packet source signal[[,]] and extracting data from the

retrieved packet source signal packets so to include at least a portion of the extracted data within the data of the packetized signal packet, recording the global identification code of the single packet source signal and at least a portion of the extracted data in the packetized signal packet.

3.   (cancelled)

4.   (currently amended) The method of claim 1 wherein each of the packetized signal packets further includes a global identification code, packet sequencing information and a data payload.

5.   (currently amended) The method of claim 4 wherein the singleat least one of the packet source signals is a video signal and wherein each packetized signal corresponding to the packet source signal includes video data and position information indicating how the video data is to be displayed on a video display.

6.   (currently amended) The method of claim 5 wherein the position information includes pixel information indicating a position within a window of the video display at which the video data is to be displayed.

7.   (cancelled)

8.   (cancelled)

9.   (currently amended) A method of producing one or more output signals from one or more input signals, the method comprising:
    (a)   receiving a plurality ofone or more input signals;
    (b)   buffering each of the input signals in an input processor memory system;

(c)   ~~processing at least one of the input signals to provide a processed signal and buffering the processed signal in the memory system;~~

~~(d)~~(c) designating at least <u>some</u> of the input signals ~~or the processed signals~~ as packet source signals and assigning each of the packet source signals a unique global identification code;

~~(e)~~(d) retrieving ~~at least one of the~~<u>one or more of the</u> packet source signals and generating ~~the~~<u>one or more</u> packetized signal<u>s</u> wherein <u>each of</u> the packetized signal<u>s</u> includes a series of packetized signal packet<u>s</u>, wherein each of the packetized signal packets contains the <u>unique</u> global identification code of one of the packet source signals and data corresponding to the same packet source signal<u>;</u>

~~(f)~~(e) transmitting the <u>one or more</u> packetized signal<u>s</u> across a communications link;

~~(g)~~(f) receiving the <u>one or more</u> packetized signals<u>;</u>

~~(h)~~(g) extracting each of the packetized signal packets from the <u>one or more</u> packetized signal<u>s</u>;

~~(i)~~(h) buffering each of the packetized signal packets containing the same <u>unique</u> global identification code in a separate data buffer in an output processor memory system and designating the packetized signal packets in each separate data buffer as an output source signal;<u> and</u>

~~(j)~~(i) producing <u>one or more</u> ~~each of the~~ output ~~source~~ signals by retrieving one or more output source signals and combining the retrieved output source signals.

10.   (currently amended) The method of claim 9 ~~wherein each of packet source signals comprises a series of packet source signal packets, and~~ wherein each of <u>the</u> packetized signal packet<u>s</u> is formed by retrieving one or more ~~the~~packet source signal packets corresponding to a single packet source signal[[,]]<u>and</u> extracting data from the retrieved <u>packet source signal</u> packets <u>so to include at least a portion of the extracted</u>

data within the data of a packetized signal packet, ~~recording the global identification~~ ~~code of the single packet source signal and at least a portion of the extracted data in the~~ ~~packetized signal packet~~.

11.   (currently amended) The method of claim 10 the ~~single~~ at least one of the packet source signal<u>s</u> is a video signal and wherein each packetized signal corresponding to the packet source signal includes video data and position information indicating how the video data is to be displayed on a video display.

12.   (cancelled)

13.   (cancelled)

14.   (currently amended) A system for receiving ~~a plurality of~~ one or more input signals and for producing ~~a plurality of~~ one or more output signals, the system comprising:

    (a)   a master controller for generating input processor control signals and output processor control signals;

    (b)   an input processor having:

        (i)   ~~a plurality of~~one or more input ports for receiving the input signals;

        (ii)   ~~a plurality of~~one or more input signal processors for processing the input signals to provide one or more processed signals

        (iii)   an input processor memory system for buffering the input signals and the processed signals, wherein at least some of the buffered signals are designated as packet source signals;

        (iv)   [[a]]one or more packetized signal output port<u>s</u>;

        (iv)   one or more packetized signal output stages for retrieving one or more of the packet source signals from the input processor memory system and for producing [[a]]one or more packetized signal<u>s</u> at the

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packetized signal output ports, wherein each of the packetized

signals includes a series of packetized signal packets, wherein

each of the packetized signal packets contains a unique global

identification code of one of the packet source signals and data

corresponding to ~~each of the retrieved~~the same packet source

signal[[s]]; and

(v) an input processor local controller for controlling the operation of at

least the signal processors and the packetized signal output stages

in response to the input processor control signals;

(c) an output processor having:

(i) [[a]]one or more packetized signal input ports for receiving the

packetized signals;

(ii) [[a]]one or more packetized signal input stages for extracting data

corresponding to each of the packet source signals from each of

the packetized signals and for storing data corresponding to each

of the packet source signals in a separate buffer in the output

processor memory system as an output source signal based on the

unique global identification code in the packetized signal packets of

each packetized signal;

(iii) [[an]]one or more output signal generators for providing one or

more output signals, each of the output signals corresponding to

one or more of the output source signals;

(iv) an[[d]] output processor local controller for controlling the operation

of the packetized signal input stages and the output signal

generators in response to the output processor control signals; and

(d) a communications link coupled between the one or more packetized signal

output ports and the one or more packetized signal input ports.

15. (cancelled)

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16.   (currently amended) The system of claim 14 wherein the signal processors include one or more video scalers for providing a scaled version of the <u>one or more</u> input signal<u>s</u> as [[a]]<u>one or more</u> processed signal<u>s</u>.

17.   (currently amended) The system of claim 14 wherein the signal processors include one or more data compression elements for providing a scaled version of the <u>one or more</u> input signal<u>s</u> as [[a]]<u>one or more</u> processed signal<u>s</u>.

18.   (original) The system of claim 14 further comprising one or more A/D converters coupled between one or more of the input ports and the input processor memory system.

19.   (original) The system of claim 17 wherein the data compression elements include one or more horizontal line filters.

20.   (original) The system of claim 17 wherein the data compression elements include one or more vertical line filters.

21.   (currently amended) An input processor comprising:
      (a)   ~~a plurality of input ports for receiving a plurality of input signals;~~
      (b)   ~~a memory system for buffering the input signals;~~
      (c)   ~~one or more signal processors for retrieving the input signals from the memory system and for processing the input signals to generate processed signals and for storing the processed signals in the memory system;~~
      (d)   ~~an output port;~~
      (e)   ~~a packetized signal output stage for retrieving one or more of the processed signals from the memory system and for generating a~~

~~packetized signal containing information from the retrieved signals and for providing the packetized signal at the output port; and~~

~~(f)   an input processor local controller for controlling the operation of the the memory system, the signal processors and the packetized signal output stage~~

(a)   one or more input ports for receiving the input signals;

(b)   one or more input signal processors for processing the input signals to provide one or more processed signals

(c)   an input processor memory system for buffering the input signals and the processed signals, wherein at least some of the buffered signals are designated as packet source signals;

(d)   one or more packetized signal output ports;

(e)   one or more packetized signal output stages for retrieving one or more of the packet source signals from the input processor memory system and for producing one or more packetized signals at the packetized signal output ports, wherein each of the packetized signals includes a series of packetized signal packets, wherein each of the packetized signal packets contains a unique global identification code of one of the packet source signals and data corresponding to the same packet source signal; and

(f)   an input processor local controller for controlling the operation of at least the signal processors and the packetized signal output stages in response to the input processor control signals.

22.   (original) The input processor of claim 21 wherein the signal processors include one or more video scalers for processing an scaled version of the input signal as a processed signal.

23.   (cancelled)

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24.   (currently amended) A method of generating one or more outgoing packetized signals from one or more incoming packetized signals, the method comprising:

(a)   receiving one or more incoming packetized signals, each of the packetized signals including a plurality of packetized signal packets identified with a unique global identification code;

(b)   ~~recording~~storing each of the packetized signal packets in a packet storage location;

(c)   recording a number of outgoing packetized signals in which each of the packetized signal packets will be included;

(d)   instructing a group of packetized signal output stages to read each of the packetized signal packets, the number of packetized signal output stage corresponding to the number recorded in (c).

25.   (currently amended) A packet router comprising:

(a)   ~~a plurality of~~one or more input stages, each of the input stages configured to receive an incoming packetized signal, determine the global identification code of each packetized signal packet extracted from the packetized signal, and store packetized signal packets ~~extracted from the packetized signal~~in a separate buffer in a packet router memory system, based on the unique global identification code in the packetized signal packets of each packetized signal;

(b)   ~~a plurality of~~one or more output stages, each of the output stages configured to read packetized signal packets from the memory system and generate an outgoing packetized signal corresponding to the packetized signal packets read by the output stage; and

(c)   a router controller for controlling the storage of the packetized signal packets in the memory system and the generation of the outgoing packetized signals in response to router control signals received from a master controller.

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26.   (currently amended) The packet router of claim 25 wherein the memory system includes a plurality of packet storage locations and wherein the router controller includes a storage location table to manage ~~the~~ usage of the packet storage locations and a global identification code distribution table to manage ~~the~~ distribution of packetized signal packets to particular output stages, and wherein the router controller is configured to instruct the input stages to store each packetized signal packet in a free packet storage location and to instruct each of the particular output stages to read the packetized signal packet from the packet storage location.

27.   (currently amended) The packet router of claim [[25]]<u>26</u> wherein the global identification code distribution table identifies the particular output stages to which <u>packetized signal packets</u>~~packets~~ having a particular global identification code are distributed.

28.   (currently amended) The packet router of claim [[25]]<u>26</u> wherein the storage location table tracks the number of output stages that require a packetized signal packet from each packet storage location and identifies a particular packet storage location as free if no output stage requires a packetized signal packet in the particular packet storage location.

29.   (new) The method of claim 1 further comprising processing at least one of the input signals to provide one or more processed signals and buffering the one or more processed signals in the memory system; and wherein said designating comprises designating at least some of the input signals or the processed signals as packet source signals.

30.   (new) The method of claim 29 wherein the processing step includes scaling at least one of the input signals to provide a processed signal.

31.　(new)　The method of claim 29 wherein the processing step includes compressing at least one of the input signals to provide a processed signal.

32.　(new)　The method of claim 9 further comprising processing at least one of the input signals to provide one or more processed signals and buffering the one or more processed signals in the input processor memory system; and wherein said designating comprises designating at least some of the input signals or the processed signals as packet source signals.

33.　(new)　The method of claim 32 wherein the processing step includes scaling at least one of the input signals to provide a processed signal.

34.　(new)　The method of claim 32 wherein the processing step includes compressing at least one of the input signals to provide a processed signal.

35.　(new)　A method of producing one or more output signals from one or more packetized signals, the method comprising:

　　(a)　receiving the one or more packetized signals, wherein each of the packetized signals includes a series of packetized signal packets, wherein each of the packetized signal packets contains a unique global identification code of a packet source signal and data corresponding to the same packet source signal;

　　(b)　extracting each of the packetized signal packets from the one or more packetized signals;

　　(c)　buffering each of the packetized signal packets containing the same unique global identification code in a separate data buffer in an output processor memory system and designating the packetized signal packets in each separate data buffer as an output source signal; and

(d)   producing one or more output signals by retrieving one or more output source signals and combining the retrieved output source signals.

36.   (new) An output processor comprising:

(a)   one or more packetized signal input ports for receiving one or more packetized signals;

(b)   one or more packetized signal input stages for extracting data corresponding to a packet source signal from each of the packetized signals and for storing data corresponding to each of the packet source signals in a separate buffer in an output processor memory system as an output source signal based on a unique global identification code in the packetized signal packets of each packetized signal;

(c)   one or more output signal generators for providing one or more output signals, each of the output signals corresponding to one or more of the output source signals; and

(d)   an output processor local controller for controlling the operation of the packetized signal input stages and the output signal generators in response to the output processor control signals.